Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 3, 6 and 16 have been amended. No claims have been cancelled. Therefore, claims 1, 3-11 and 16-22 are presented for examination.

In the Office Action, claims 1 and 3-5 stand rejected under 35 U.S.C. §102(b) as being anticipated by Barenys et al. (U.S. Patent No. 6,145,036). Applicant submits that the present claims are patentable over Barenys.

Barenys discloses an expansion processor that resides on a primary I^2C bus, which includes a primary SDA and a primary SCL. The expansion processor may be an I^2C slave responding to requests from an I^2C bus master residing on a primary I^2C bus. A bus master on a primary bus may initiate requests for an I^2C transaction (either a read or a write) to a plurality of expansion devices. These expansion devices may include any I^2C compatible device, and may include, but are not necessarily limited to, microprocessors, gate arrays, liquid crystal display (LCD) drivers, memory, data converters, network drivers/adapters, and application oriented devices. See Barenys at col. 3, ll. 11-30. Barenys further discloses that the expansion processor may be implemented in a memory chip having the expansion processor connected to a primary bus. The memory chip contains a plurality of memory modules (e.g., DIMMs). Each of these DIMMs is connected by an I^2C sub-bus to the expansion processor. If a DIMM fails, only its particular sub-bus will fail, resulting in the other sub-buses not failing and correspondingly, no failure in the primary bus 203 (col. 3, ll. 40-62).

Claim 1 of the present application recites a first management bus, directly coupled to each of a first set of field replaceable units. The Examiner cites "[m]emory chip 501

contains a plurality of memory modules 502-509, which may be dual in-line memory modules (DIMM)" (col. 3, ll. 43-54) from Barenys as disclosing such a feature. However, nowhere does Barenys disclose or suggest a first management bus, directly coupled to each of a first set of field replaceable units. A memory chip containing a plurality of memory modules is not equivalent to a first management bus, directly coupled to each of a first set of field replaceable units. In addition, DIMMs are not the same as field replaceable units. Therefore, claim 1 is patentable over Barenys.

Claims 3-5 depend from claim 1 and include additional features. Thus, claims 3-5 are also patentable over Barenys.

Claims 1, 3-11, and 16-21 stand rejected under 35 U.S.C. §102(e) as being anticipated by Holland et al. (U.S. Patent No. 5,367,669). Applicant submits that the present claims are patentable over Holland.

Holland discloses a microcontroller system which contains a microcontroller with standard microcontroller peripherals. The microcontroller system receives pulses into its digital in ports from fans indicating rotational frequency of the fans, and it uses analog-to-digital converters (ADCs) to monitor the voltages of power supplies. It also uses ADCs to monitor input from temperature sensors that are located at various points in a single chassis. See Holland at col. 8, ll. 38-48.

Claim 1 of the present application recites a first management bus, directly coupled to each of a first set of field replaceable units. Applicant submits that Holland does not disclose or suggest such a feature. The microcontroller receiving pulses indicating rotational frequency of fans, monitoring voltage of power supplies, and monitoring temperature

sensors, is not equivalent to a first management bus, directly coupled to each of a first set of field replaceable units. Therefore, claim 1 is patentable over Holland.

Claims 3-5 depend from claim 1 and include additional features. Thus, claims 3-5 are also patentable over Holland.

Claim 6 recites a first management bus, directly coupled to each of a first set of field replaceable units. For the reasons described above with respect to claim 1, claim 6 is patentable over Holland. Since claims 7-11 depend from claim 6 and include additional features, claims 7-11 are also patentable over Holland.

Claim 16 recites a first management bus directly coupled to each of the two or more temperature sensors. For the reasons described above with respect to claim 1, claim 16 is also patentable over Holland. Because claims 17-22 depend from claim 16 and include additional features, claims 17-22 are also patentable over Holland.

Claim 22 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Holland (U.S. Patent No. 5,367,669), in view of Jewett et al. (U.S. Patent No. 6,073,251). Applicant submits that the present claims are patentable over Holland in view of Jewett.

Jewett discloses a computer system in a fault tolerant configuration that employs multiple identical CPUs executing the same instruction stream. See Jewett at Abstract. However, Jewett fails to disclose or suggest a first management bus, directly coupled to each of a first set of field replaceable units.

As discussed above, Holland does not disclose or suggest such a feature. Since neither Holland nor Jewett disclose or suggest a first management bus, directly coupled to each of a first set of field replaceable units, any combination of Holland and Jewett would

not disclose or suggest the feature. Therefore, claim 22 is patentable over Holland in view of Jewett.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: November 14, 2005

Mark L. Watson
Reg. No. 46,322

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980